

## 0.75-Ω SPDT ANALOG SWITCH WITH INPUT LOGIC TRANSLATION

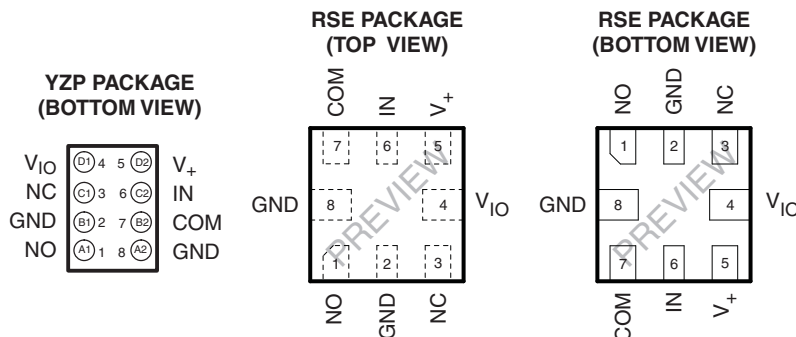
### FEATURES

- Specified Break-Before-Make Switching
- Low ON-State Resistance (0.75 Ω Max)
- Control Inputs Referenced to  $V_{IO}$
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 2.25-V to 5.5-V Power Supply ( $V_+$ )
- 1.65-V to 1.95-V Logic Supply ( $V_{IO}$ )
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 4000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
  - 400-V (YZP Package) / 250-V (RSE Package) Machine Model (A115-A)

- COM Port to GND
  - 8000-V Human-Body Model (A114-B, Class II)
  - ±15-kV Contact Discharge (IEC 61000-4-2)

### APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation



### DESCRIPTION/ORDERING INFORMATION

The TS5A6542 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 2.25 V to 5.5 V. The device offers a low ON-state resistance with an excellent channel-to-channel ON-state resistance matching, and the break-before-make feature to prevent signal distortion during the transferring of a signal from one path to another. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

The TS5A6542 has a separate logic supply pin ( $V_{IO}$ ) that is characterized to operate from 1.65 V to 1.95 V.  $V_{IO}$  powers the control circuitry, which allows the TS5A6542 to be controlled by 1.8-V signals.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**ORDERING INFORMATION**

$T_A$	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	TS5A6542YZPR	___ JH7
	QFN – RSE	Tape and reel	TS5A6542RSER	PREVIEW

- (1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).  
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).  
(3) YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

**SUMMARY OF CHARACTERISTICS<sup>(1)</sup>**

Configuration	2:1 Multiplexer/Demultiplexer (1 × SPDT)
Number of channels	1
ON-state resistance ( $r_{on}$ )	0.75 $\Omega$ max
ON-state resistance match ( $\Delta r_{on}$ )	0.1 $\Omega$ max
ON-state resistance flatness ( $r_{on(flat)}$ )	0.1 $\Omega$ max
Turn-on/turn-off time ( $t_{ON}/t_{OFF}$ )	25 ns/20 ns
Charge injection ( $Q_C$ )	15 pC
Bandwidth (BW)	43 MHz
OFF isolation ( $O_{ISO}$ )	–63 dB at 1 MHz
Crosstalk ( $X_{TALK}$ )	–63 dB at 1 MHz
Total harmonic distortion (THD)	0.004%
Leakage current ( $I_{NO(OFF)}/I_{NC(OFF)}$ )	20 nA
Package option	8-pin WCSP

(1)  $V_+ = 5$  V,  $T_A = 25^\circ\text{C}$

**FUNCTION TABLE**

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

## ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_+$ $V_{IO}$	Supply voltage range <sup>(3)</sup>	–0.5	6.5	V
$V_{NC}$ $V_{NO}$ $V_{COM}$	Analog voltage range <sup>(3)(4)(5)</sup>	–0.5	$V_+ + 0.5$	V
$I_{I/OK}$	Analog port diode current <sup>(6)</sup>	$V_{NO}, V_{COM} < 0$ or $V_{NO}, V_{COM} > V_+$		mA
$I_{INC}$ $I_{INO}$ $I_{COM}$	On-state switch current	–200	200	mA
	On-state peak switch current <sup>(7)</sup>	–400	400	
$V_I$	Digital input voltage range <sup>(3)(4)</sup>	–0.5	6.5	V
$I_{IK}$	Digital input clamp current	$V_I < 0$		mA
$I_+$ $I_{GND}$	Continuous current through $V_+$ or GND	–100	100	mA
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Requires clamp diodes on analog port to  $V_+$ .
- (7) Pulse at 1-ms duration < 10% duty cycle

## THERMAL IMPEDANCE RATINGS

		UNIT	
$\theta_{JA}$	Package thermal impedance <sup>(1)</sup>	RSE package	TBD
		YZP package	102

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

**ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY<sup>(1)</sup>**
 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $V_{IO} = 1.65 \text{ V to } 1.95 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V
ON-state resistance	$r_{on}$	$V_{NO}$ or $V_{NC} = 2.5 \text{ V}$ , $I_{COM} = -100 \text{ mA}$ , Switch ON, See Figure 14	25°C Full	4.5 V		0.5	0.75 0.8	$\Omega$
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO}$ or $V_{NC} = 2.5 \text{ V}$ , $I_{COM} = -100 \text{ mA}$ , Switch ON, See Figure 14	25°C Full	4.5 V		0.05	0.1 0.1	$\Omega$
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100 \text{ mA}$ , Switch ON, See Figure 14  $V_{NO}$ or $V_{NC} = 1 \text{ V}$ , 1.5 V, 2.5 V, $I_{COM} = -100 \text{ mA}$ , Switch ON, See Figure 14	25°C Full	4.5 V		0.1	0.1 0.25 0.25	$\Omega$
NO, NC OFF leakage current	$I_{NO(OFF)}, I_{NC(OFF)}$	$V_{NO} = 1 \text{ V}, 4.5 \text{ V}$ , $V_{COM} = 4.5 \text{ V}, 1 \text{ V}$ , $V_{NC} = \text{Open}$ , or $V_{NO} = 1 \text{ V}, 4.5 \text{ V}$ , $V_{COM} = 4.5 \text{ V}, 1 \text{ V}$ , $V_{NO} = \text{Open}$ , Switch OFF, See Figure 15	25°C Full	5.5 V	-20	2	20 100	nA
NC, NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1 \text{ V}, 4.5 \text{ V}$ , $V_{COM}, V_{NC} = \text{Open}$ , or $V_{NC} = 1 \text{ V}, 4.5 \text{ V}$ , $V_{COM}, V_{NO} = \text{Open}$ , Switch ON, See Figure 16	25°C Full	5.5 V	-20	2	20 200	nA
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1 \text{ V}, 4.5 \text{ V}$ , $V_{NO}$ and $V_{NC} = \text{Open}$ , or $V_{COM} = 1 \text{ V}, 4.5 \text{ V}$ , $V_{NO}$ or $V_{NC} = \text{Open}$ , See Figure 16	25°C Full	5.5 V	-20	2	20 200	nA
<b>Digital Control Input (IN)<sup>(2)</sup></b>								
Input logic high	$V_{IH}$	$V_{IO} = 1.65 \text{ V to } 1.95 \text{ V}$	Full		$0.65 \times V_{IO}$		$V_{IO}$	V
Input logic low	$V_{IL}$	$V_{IO} = 1.65 \text{ V to } 1.95 \text{ V}$	Full		0		$0.35 \times V_{IO}$	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = V_{IO}$ or 0	25°C Full	5.5 V	-2		2 20	nA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_{IO}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY (continued)**
 $V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{IO} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	5 V	1	12.5	25	ns
				Full	4.5 V			30	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	5 V	1	9.5	20	ns
				Full	4.5 V			25	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+/2$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	5 V	1	5	10	ns
				Full	4.5 V	1		12	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See <a href="#">Figure 23</a>	25°C	5 V		15	pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 17</a>	25°C	5 V		37	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	5 V		130	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	5 V		130	pF	
Digital input capacitance	$C_I$	$V_I = V_{IO}$ or GND,	See <a href="#">Figure 17</a>	25°C	5 V		6.5	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See <a href="#">Figure 20</a>	25°C	5 V		43	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	See <a href="#">Figure 21</a>	25°C	5 V		-63	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	See <a href="#">Figure 22</a>	25°C	5 V		-63	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	5 V		0.00 4	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_{IO}$ or GND	25°C	5.5 V		5.5	100	nA	
			Full				750		

**ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY<sup>(1)</sup>**
 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $V_{IO} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V	
ON-state resistance	$r_{on}$	$V_{NO}$ or $V_{NC} = 2\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 14</a>	25°C	3 V	0.75	0.9	$\Omega$	
				Full		1.2			
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO}$ or $V_{NC} = 2\text{ V}, 0.8\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 14</a>	25°C	3 V	0.1	0.15	$\Omega$	
				Full		0.15			
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 14</a>	25°C	3 V	0.2		$\Omega$	
				25°C		0.1	0.3		
				Full		0.3			
NO, NC OFF leakage current	$I_{NO(OFF)}, I_{NC(OFF)}$	$V_{NO} = 1\text{ V}, 3\text{ V}$ , $V_{COM} = 3\text{ V}, 1\text{ V}$ , $V_{NC} = \text{Open}$ , or $V_{NC} = 1\text{ V}, 3\text{ V}$ , $V_{COM} = 3\text{ V}, 1\text{ V}$ , $V_{NO} = \text{Open}$ ,	Switch OFF, See <a href="#">Figure 15</a>	25°C	3.6 V	-20	2	20	nA
				Full		-50		50	
NC, NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1\text{ V}, 3\text{ V}$ , $V_{NC}$ and $V_{COM} = \text{Open}$ , or $V_{NC} = 1\text{ V}, 3\text{ V}$ , $V_{NO}$ and $V_{COM} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 16</a>	25°C	3.6 V	-10	2	10	nA
				Full		-30		30	
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$ , $V_{NO}$ and $V_{NC} = \text{Open}$ , or $V_{COM} = 3\text{ V}$ , $V_{NO}$ and $V_{NC} = \text{Open}$ ,	See <a href="#">Figure 16</a>	25°C	3.6 V	-10	2	10	nA
				Full		-30		30	
<b>Digital Control Input (IN)<sup>(2)</sup></b>									
Input logic high	$V_{IH}$	$V_{IO} = 1.65\text{ V to }1.95\text{ V}$		Full		$0.65 \times V_{IO}$	$V_{IO}$	V	
Input logic low	$V_{IL}$	$V_{IO} = 1.65\text{ V to }1.95\text{ V}$		Full		0	$0.35 \times V_{IO}$	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = V_{IO}$ or 0		25°C	3.6 V	-2	2	nA	
				Full		-20	20		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_{IO}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY (continued)**
 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $V_{IO} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	3.3 V	5	15	30	ns
				Full	3 V	3		35	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	3.3 V	1	9	20	ns
				Full	3 V	1		25	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+/2$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	3.3 V	1	8	13	ns
				Full	3 V	1		15	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See <a href="#">Figure 23</a>	25°C	3.3V		6.5	pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 17</a>	25°C	3.3 V		38	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	3.3 V		133	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	3.3 V		133	pF	
Digital input capacitance	$C_I$	$V_I = V_{IO}$ or GND,	See <a href="#">Figure 17</a>	25°C	3.3 V		6.5	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See <a href="#">Figure 20</a>	25°C	3.3 V		42	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	See <a href="#">Figure 21</a>	25°C	3.3 V		-63	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	See <a href="#">Figure 22</a>	25°C	3.3 V		-63	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	3.3 V		0.00 4	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_{IO}$ or GND	25°C	3.6 V		10	50	nA	
			Full				300		

**Electrical Characteristics for 2.5-V Supply<sup>(1)</sup>**

$V_+ = 2.25\text{ V to }2.75\text{ V}$ ,  $V_{IO} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V	
ON-state resistance	$r_{on}$	$V_{NO}$ or $V_{NC} = 1.8\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 14</a>	25°C	2.25 V	1	1.3	$\Omega$	
				Full		1.6			
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO}$ or $V_{NC} = 1.8\text{ V}$ , 0.8 V, $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 14</a>	25°C	2.25 V	0.15	0.2	$\Omega$	
				Full		0.2			
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 14</a>	25°C	2.25 V	0.5		$\Omega$	
				25°C		0.25			
				Full		0.6			
NO, NC OFF leakage current	$I_{NO(OFF)}, I_{NC(OFF)}$	$V_{NO} = 0.5\text{ V}, 2.2\text{ V}$ , $V_{COM} = 2.2\text{ V}, 0.5\text{ V}$ , $V_{NC} = \text{Open}$ , or $V_{NC} = 0.5\text{ V}, 2.2\text{ V}$ , $V_{COM} = 2.2\text{ V}, 0.5\text{ V}$ , $V_{NO} = \text{Open}$ ,	Switch OFF, See <a href="#">Figure 15</a>	25°C	2.75 V	-20	2	20	nA
				Full		-50		50	
NC, NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 0.5\text{ V}, 2.2\text{ V}$ , $V_{NC}$ and $V_{COM} = \text{Open}$ , or $V_{NC} = 2.2\text{ V}, 0.5\text{ V}$ , $V_{NO}$ and $V_{COM} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 16</a>	25°C	2.75 V	-10	2	10	nA
				Full		-20		20	
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 0.5\text{ V}$ , $V_{NO}$ and $V_{NC} = \text{Open}$ , or $V_{COM} = 2.2\text{ V}$ , $V_{NO}$ and $V_{NC} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 16</a>	25°C	2.75 V	-10	2	10	nA
				Full		-20		20	
<b>Digital Control Input (IN)<sup>(2)</sup></b>									
Input logic high	$V_{IH}$	$V_{IO} = 1.65\text{ V to }1.95\text{ V}$	Full		$0.65 \times V_{IO}$		$V_{IO}$	V	
Input logic low	$V_{IL}$	$V_{IO} = 1.65\text{ V to }1.95\text{ V}$	Full		0	$0.35 \times V_{IO}$		V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = V_{IO}$ or 0	25°C	2.75 V	-2		2	nA	
			Full		-20		20		

- (1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (2) All unused digital inputs of the device must be held at  $V_{IO}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**Electrical Characteristics for 2.5-V Supply (continued)**
 $V_+ = 2.25\text{ V to }2.75\text{ V}$ ,  $V_{IO} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	2.5 V	5	20	35	ns
				Full	2.25 V	5		40	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	2.5 V	2	10	20	ns
				Full	2.25 V	2		25	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+/2$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	2.5 V	1	11	20	ns
				Full	2.25 V	1		25	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See <a href="#">Figure 23</a>	25°C	2.5 V		5	pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 17</a>	25°C	2.5 V		38	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	2.5 V		135	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	2.5 V		135	pF	
Digital input capacitance	$C_I$	$V_I = V_{IO}$ or GND,	See <a href="#">Figure 17</a>	25°C	2.5 V		6.5	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See <a href="#">Figure 20</a>	25°C	2.5 V		40	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	See <a href="#">Figure 21</a>	25°C	2.5 V		-63	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	See <a href="#">Figure 22</a>	25°C	2.5 V		-63	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	2.5 V		0.00 8	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_{IO}$ or GND	25°C	2.75 V		10	25	nA	
			Full				100		

TYPICAL PERFORMANCE

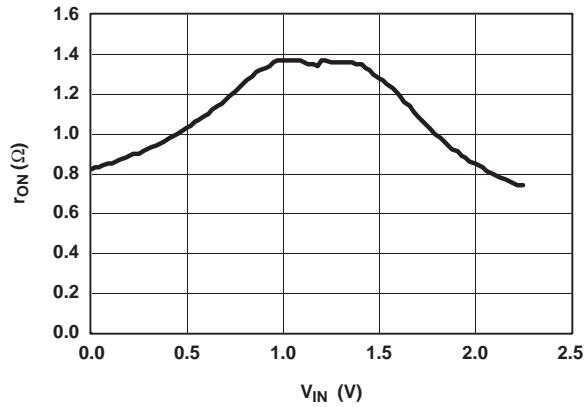


Figure 1.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 2.5$  V)

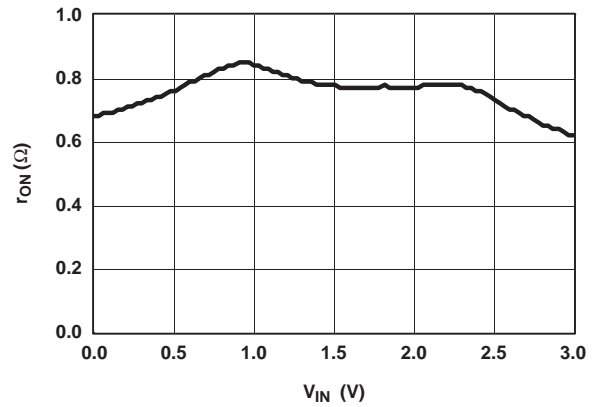


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3.3$  V)

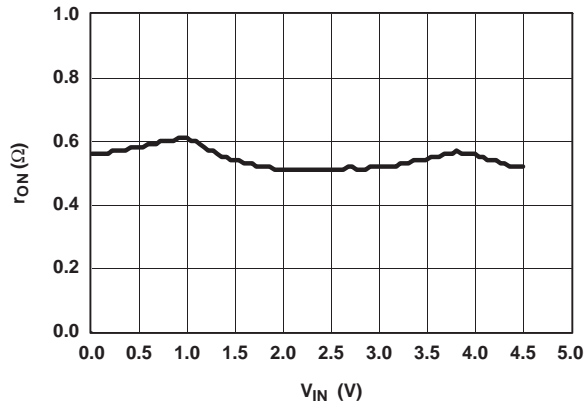


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 5$  V)

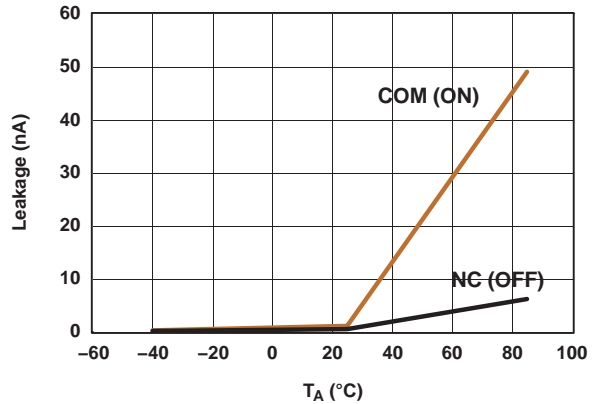


Figure 4. Leakage Current vs Temperature ( $V_+ = 5$  V)

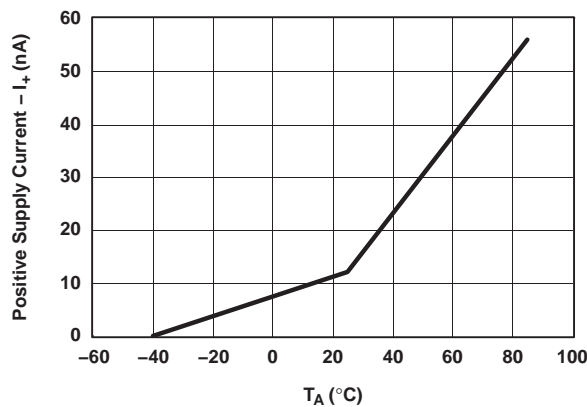


Figure 5.  $I_+$  vs Temperature ( $V_+ = 5$  V)

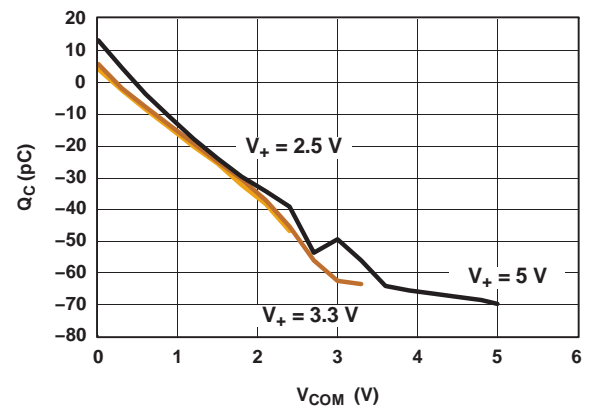


Figure 6. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

TYPICAL PERFORMANCE (continued)

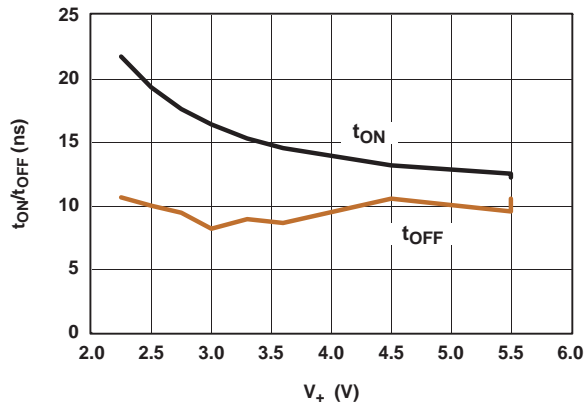


Figure 7. t<sub>ON</sub>/t<sub>OFF</sub> vs Supply Voltage

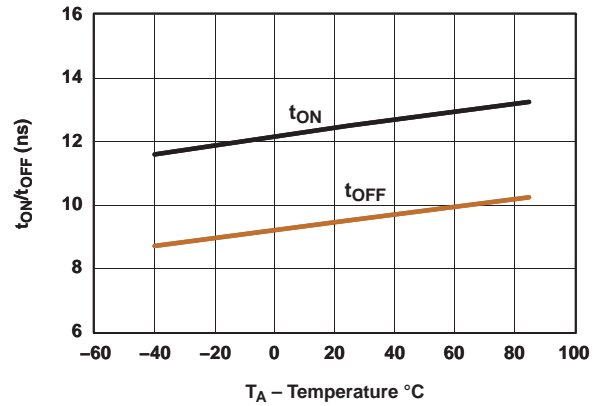


Figure 8. t<sub>ON</sub>/t<sub>OFF</sub> vs Temperature (V<sub>+</sub> = 5 V)

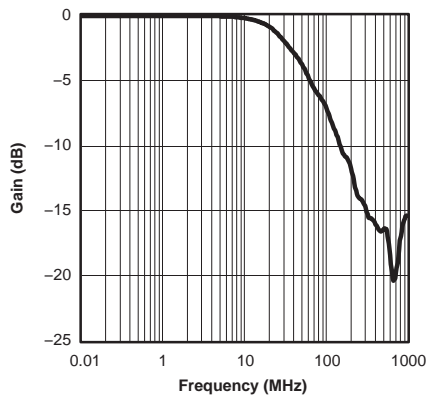


Figure 9. Gain vs Frequency (V<sub>+</sub> = 5 V)

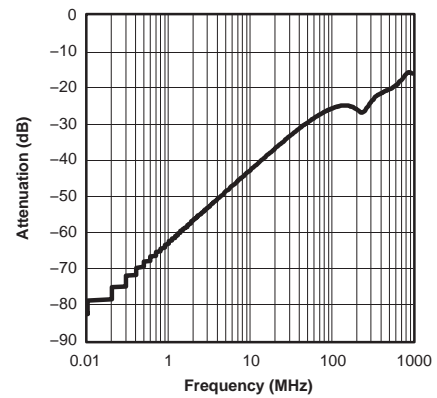


Figure 10. Crosstalk vs Frequency (V<sub>+</sub> = 5 V)

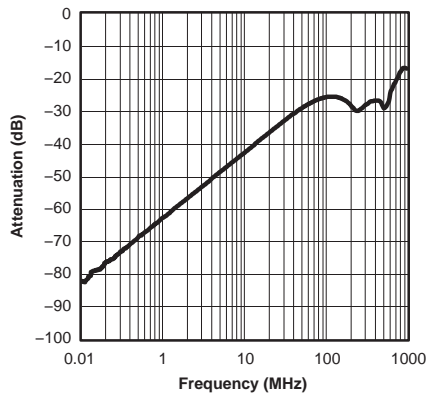


Figure 11. OFF Isolation vs Frequency (V<sub>+</sub> = 5 V)

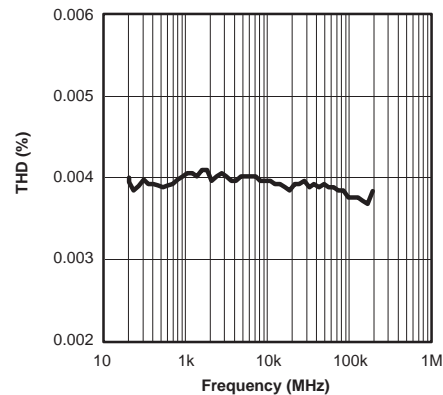
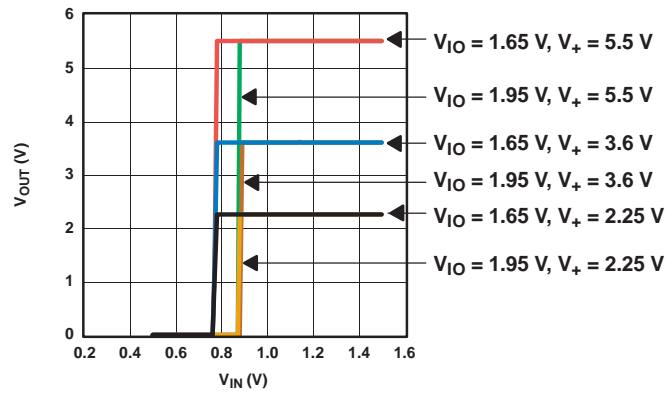


Figure 12. Total Harmonic Distortion vs Frequency (V<sub>+</sub> = 2.5 V)

**TYPICAL PERFORMANCE (continued)**



**Figure 13. V<sub>IO</sub> Thresholds**

PARAMETER MEASUREMENT INFORMATION

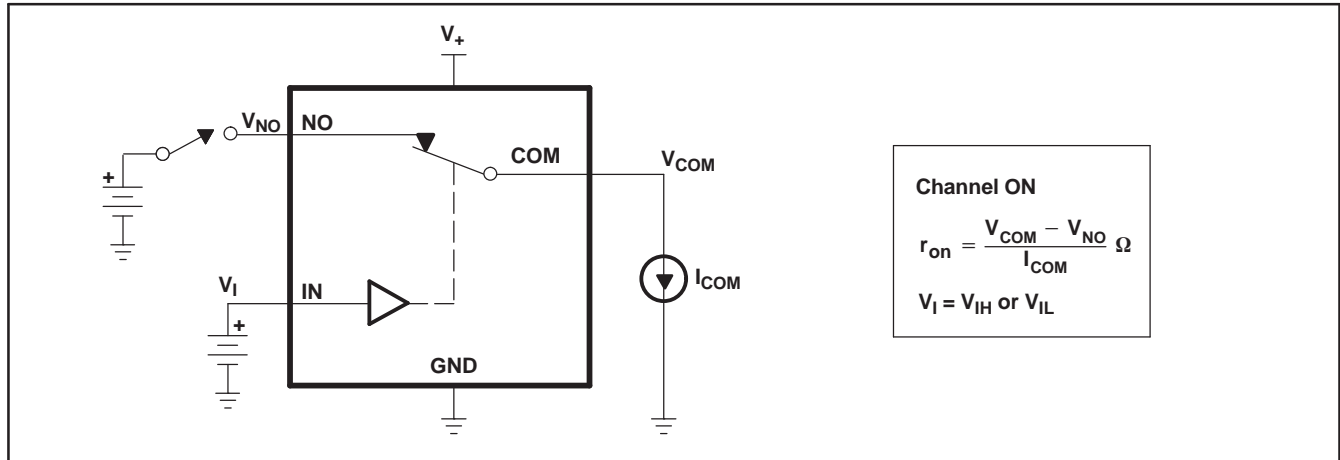


Figure 14. ON-State Resistance ( $r_{on}$ )

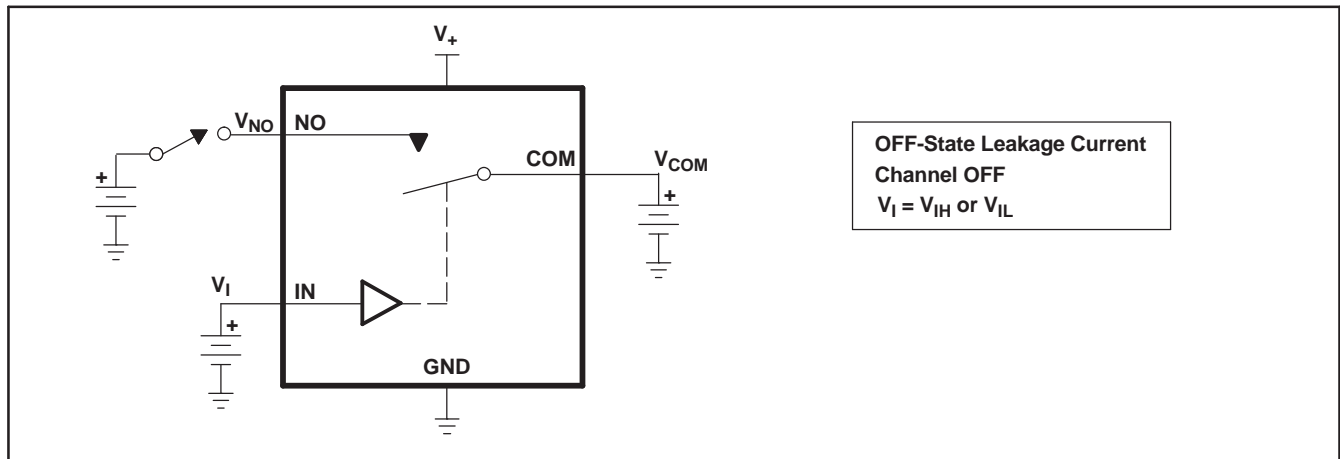


Figure 15. OFF-State Leakage Current ( $I_{COM(OFF)}$ ,  $I_{NC(OFF)}$ ,  $I_{COM(PWROFF)}$ ,  $I_{NC(PWRFF)}$ )

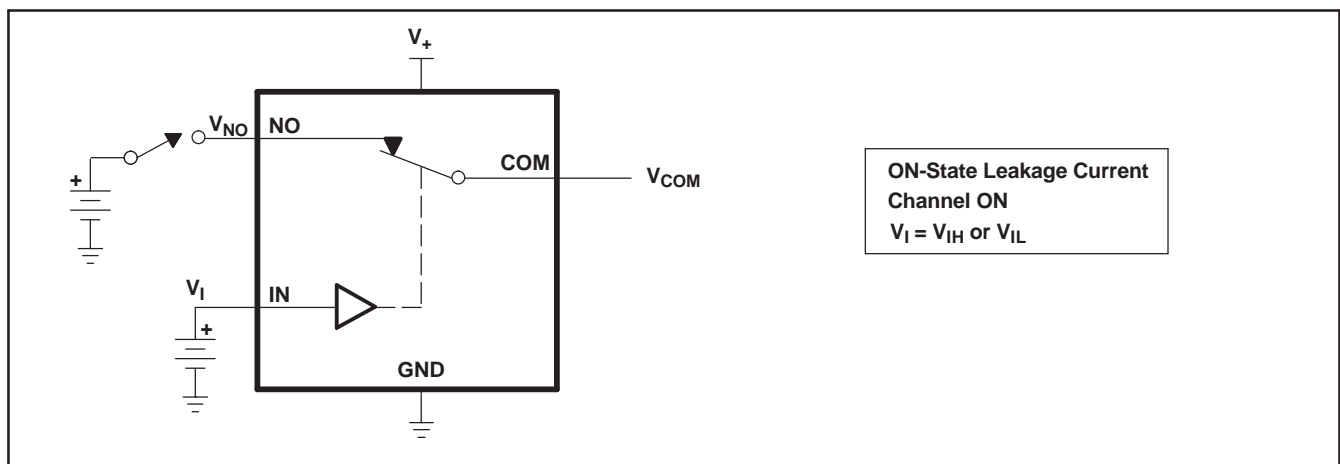


Figure 16. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ )

PARAMETER MEASUREMENT INFORMATION (continued)

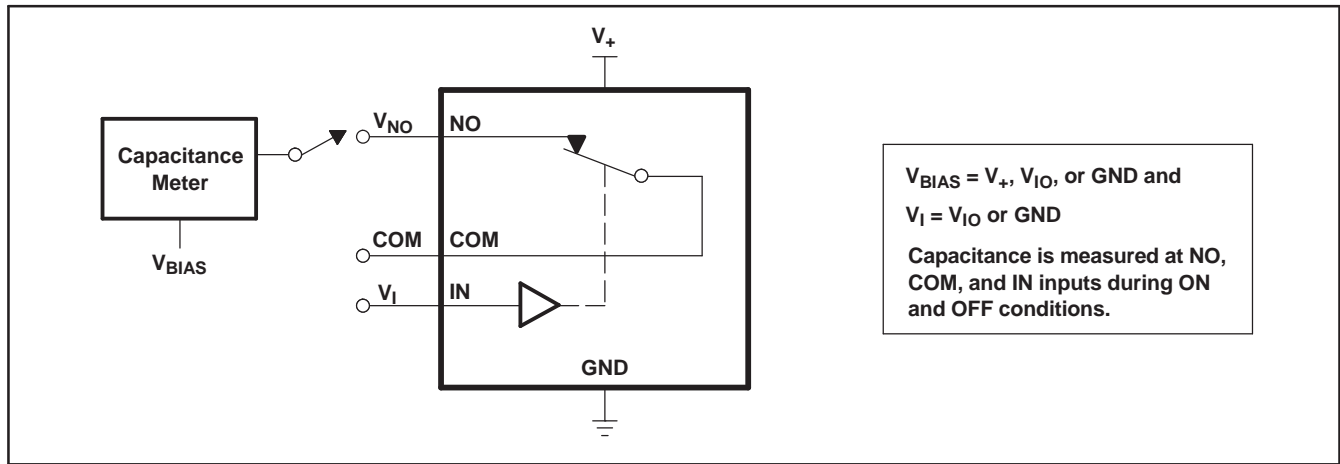
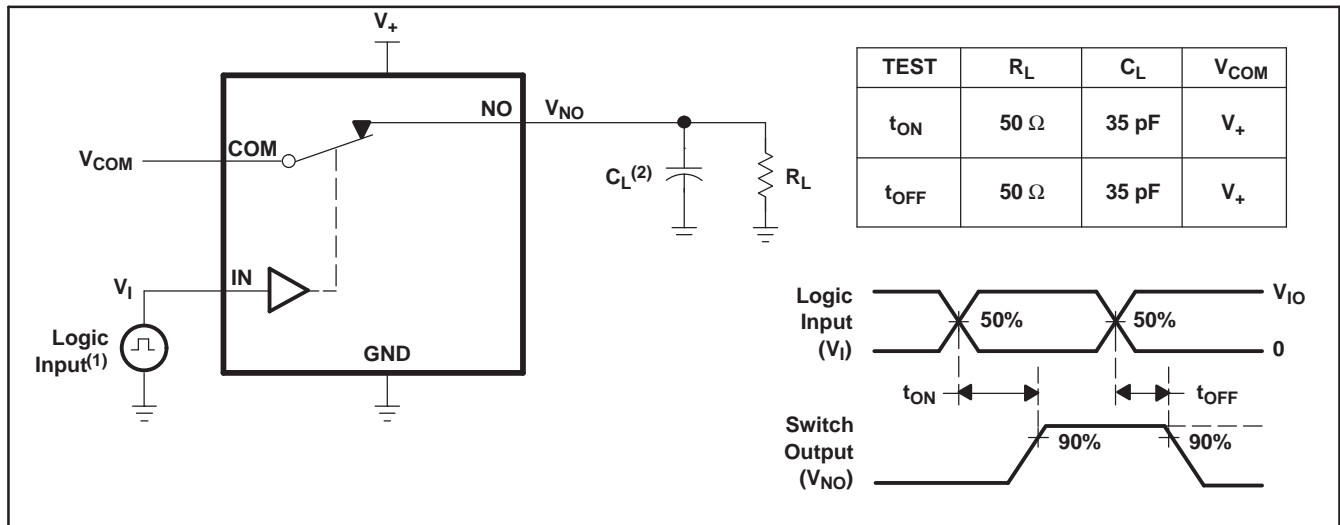


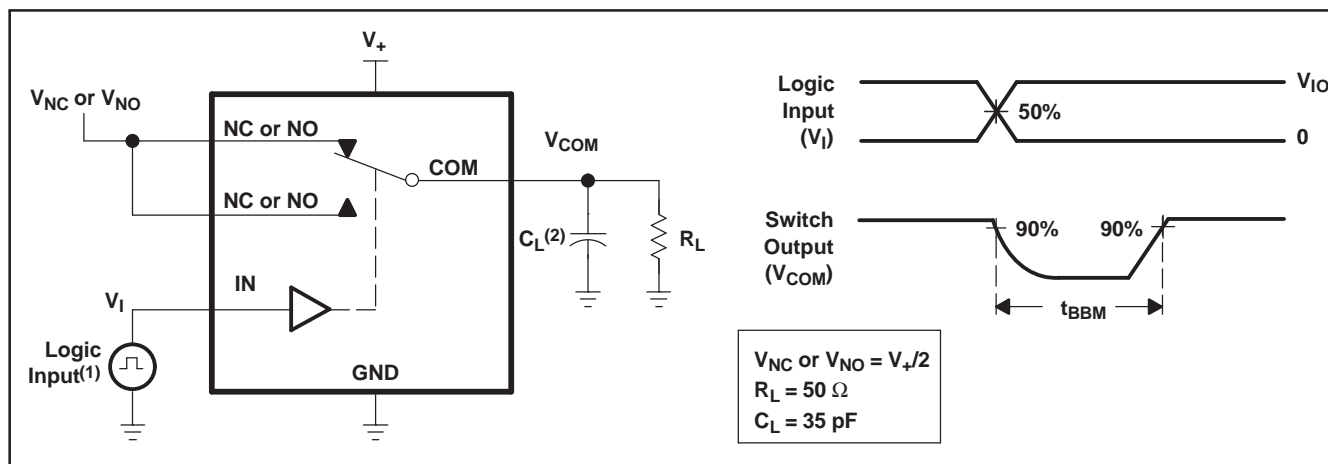
Figure 17. Capacitance ( $C_I$ ,  $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NC(OFF)}$ ,  $C_{NC(ON)}$ )



(1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.  
 (2)  $C_L$  includes probe and jig capacitance.

Figure 18. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )

PARAMETER MEASUREMENT INFORMATION (continued)



- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .  
 (2)  $C_L$  includes probe and jig capacitance.

Figure 19. Break-Before-Make Time ( $t_{BBM}$ )

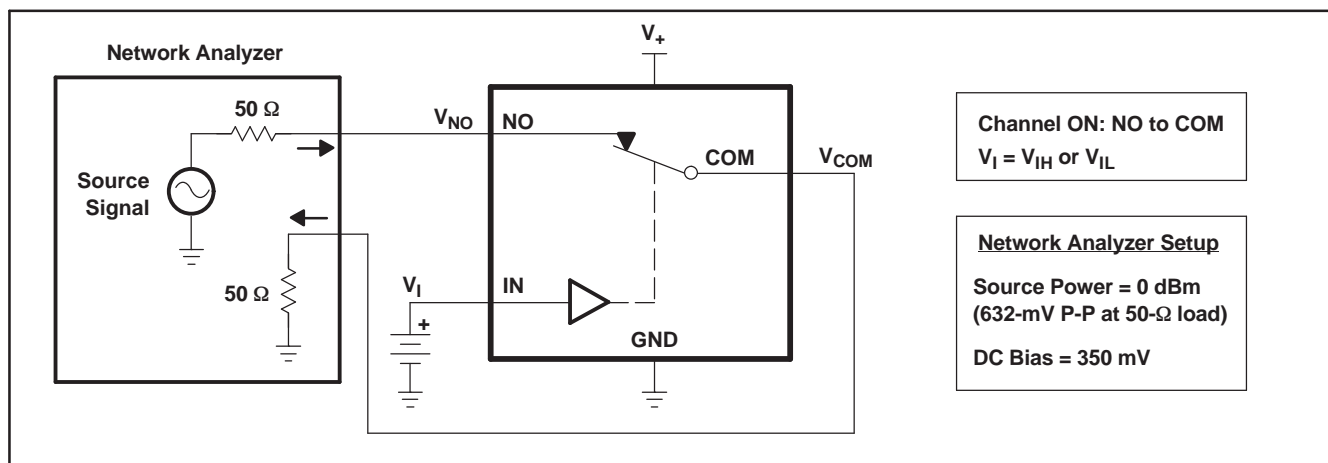


Figure 20. Bandwidth (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

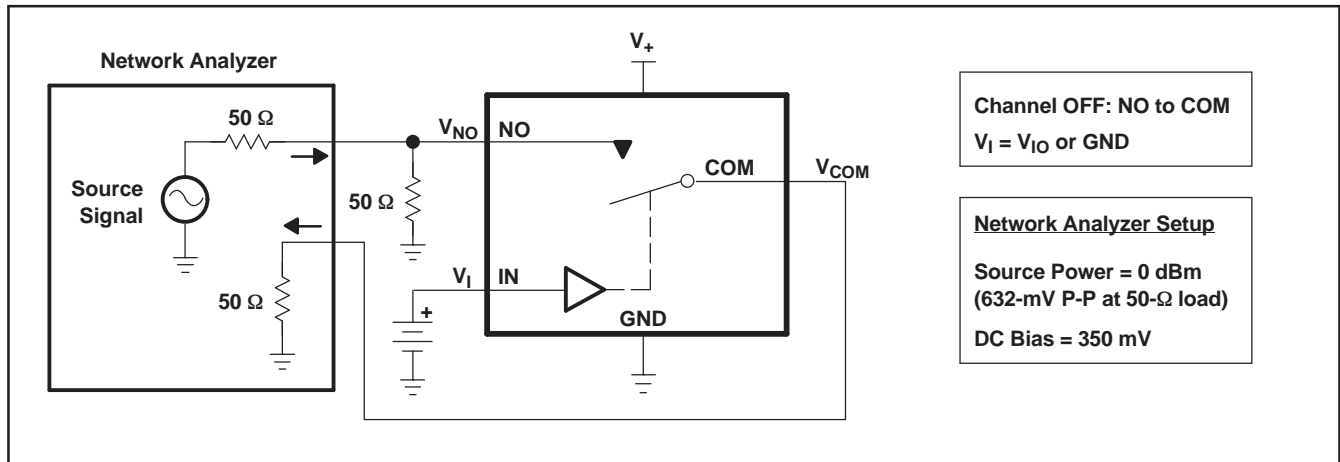


Figure 21. OFF Isolation ( $O_{ISO}$ )

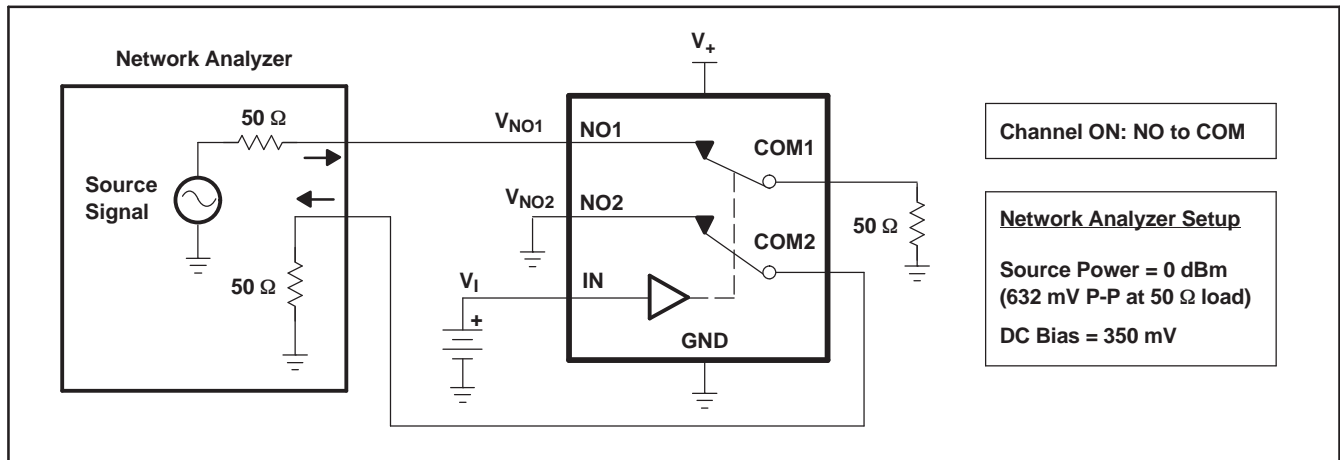
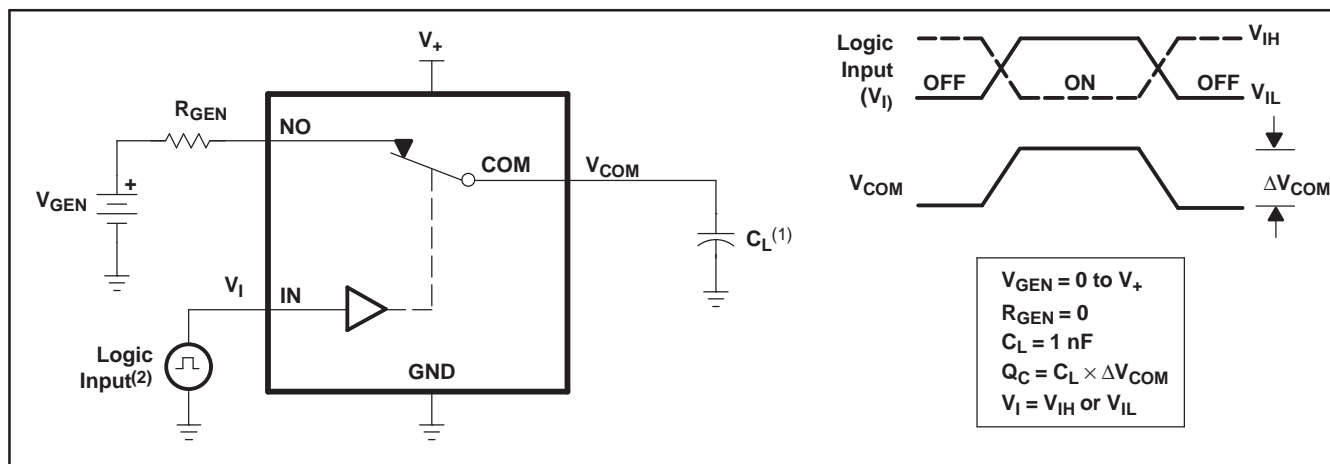


Figure 22. Crosstalk ( $X_{TALK}$ )



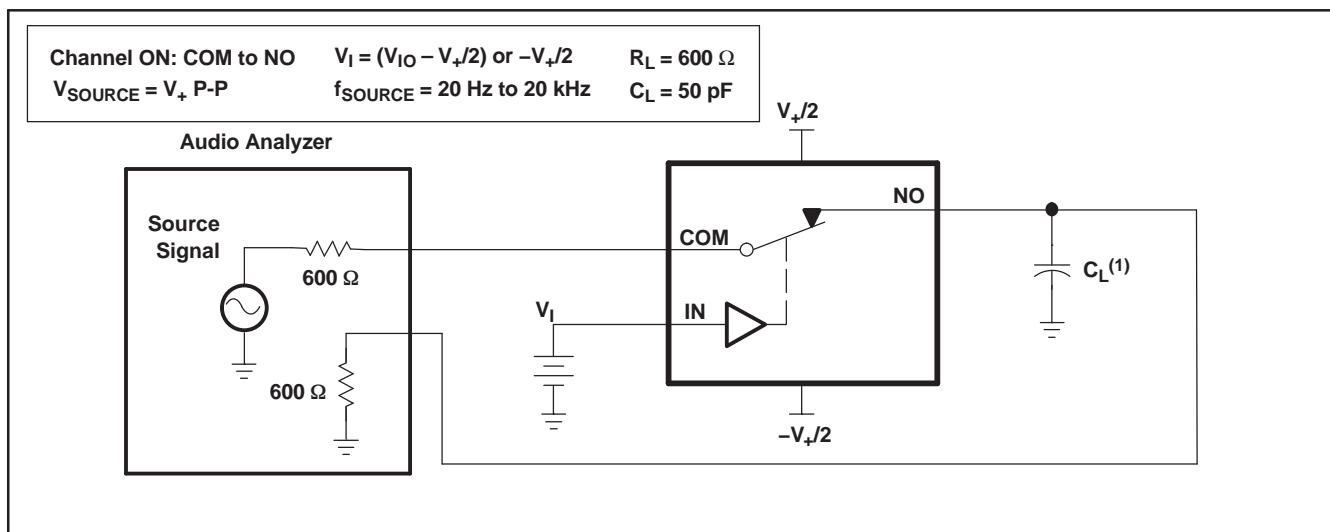
PARAMETER MEASUREMENT INFORMATION (continued)



(1)  $C_L$  includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .

Figure 23. Charge Injection ( $Q_C$ )



(1)  $C_L$  includes probe and jig capacitance.

Figure 24. Total Harmonic Distortion (THD)

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TS5A6542YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

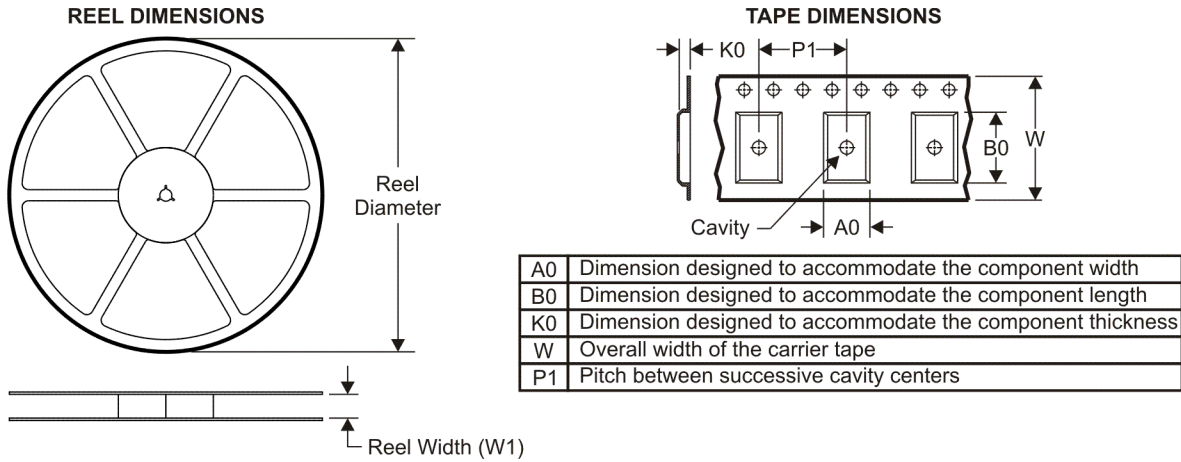
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

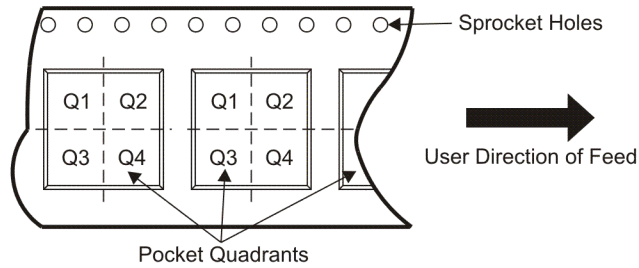
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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A6542YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.1	2.1	0.56	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

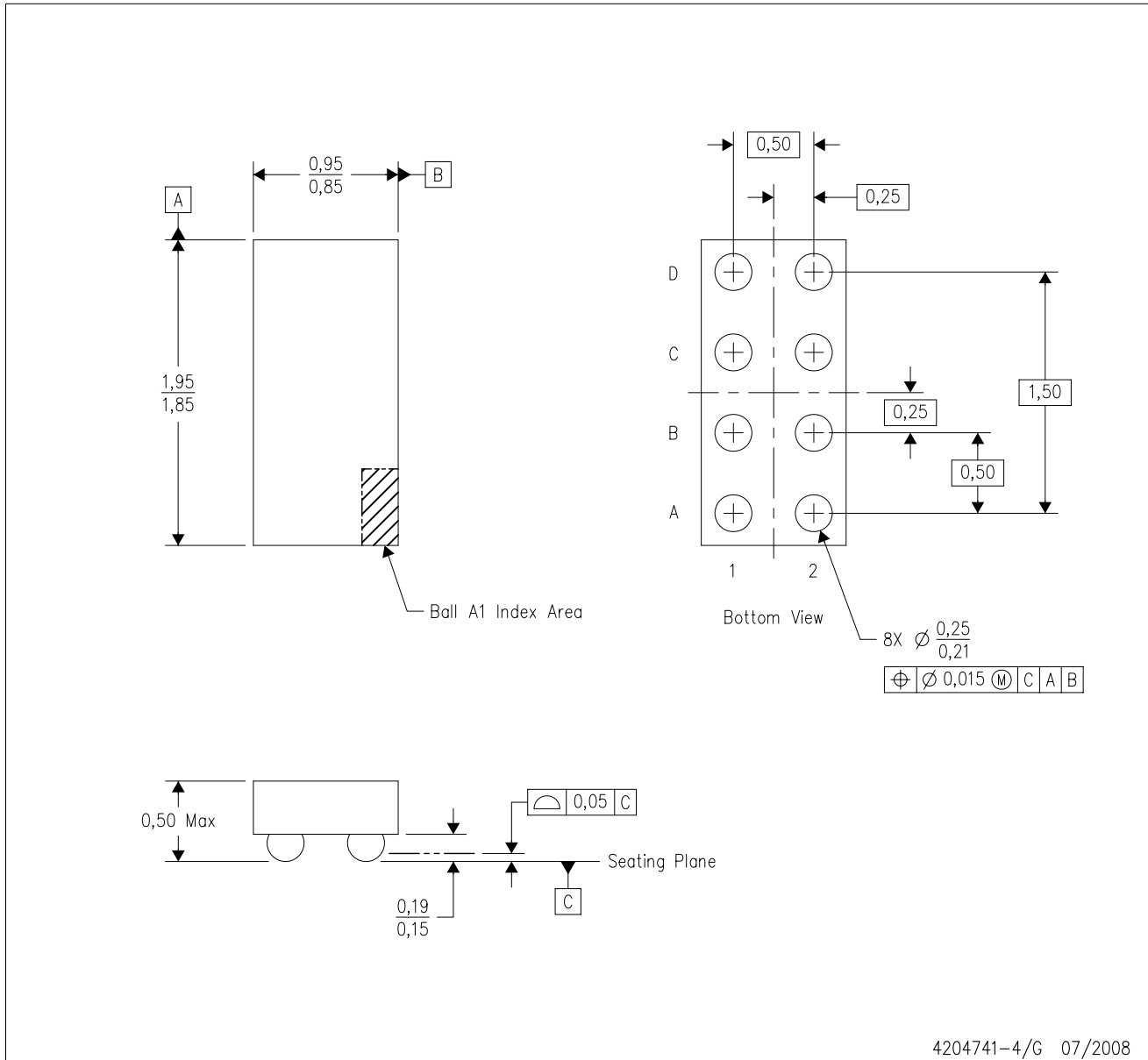


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A6542YZPR	DSBGA	YZP	8	3000	220.0	220.0	34.0

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - D. This package is lead-free. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

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